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information on the
compile ultra command
consult the Design
Compiler User Guide
(dc-user-guide.pdf) or
use `man compile ultra`
at the DC shell prompt.
Run the following
command and take a
look at the output. DC
will attempt to
synthesize your design
while

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Training Course of
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Zero button for DC, AC
magnetic function
Separate probe for
remote measurements
High accuracy
Advanced functionality
with programmable
user Settings Ideal for
a variety of laboratory
and field uses Heavy
duty, compact housing
with hard-shell carrying
case

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```
unix> dc_shell-t. Step  
1. Setup technology  
library. To synthesize a  
design you need  
technology library  
which will contain  
description of the cells  
from the fab, and their  
timing. This is usually a  
.db file found in library  
installation directory.  
To do this 1(a). Tell  
synopsys where your  
<library>.db file is.
```

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settings can be in ...

Comments? E-mail
your comments about
Synopsys
documentation to
doc@synopsys.com
Design Compiler User
Guide Version 2000.05,
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output from a shell
command back into
dc_shell (i.e. there is

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nothing analogous to using backquote in the shell for command substitution) 5 . You might think that you could set an environment variable in sh, and then use `get_unix_variable` to

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For use in `dc_shell-t` (Tcl mode of `dc_shell`) only. `string acs_get_parent_partition`

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design_name
[-hierarchy] [-list]
acs_get_path (dctcl-
mode only) Gets the
path location for the
specified file. To
specify a file, specify
its file type and, for
pass-dependent files,
its pass directory. For
use in dc_shell-t (Tcl
mode of dc_shell) only
...

[Linux dc command
help and examples -
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This guide describes the AC/DC Module, an optional add-on package for COMSOL Multiphysics ® designed to assist you to solve and model low-frequency electromagnetics.

Automated Synthesis
from HDL models

View Dc_shell
commands from
ELECTRONICS 121 at
Rajasthan Technical
University. # #Design

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Compiler settings can be in

```
.synopsys_dc.setup #  
#Reading design file  
read_verilog  
golden_arbiter.v  
#Pointing
```

The AC/DC Module User's Guide - COMSOL Multiphysics

DC User Guide DC
Command Line ... Main
advantage over
dc_shell is to view the
synthesized schematic.
Synthesis stages and

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commands . Load tech
libraries. into database.
Read, analyze &
elaborate design.
Define design.
environment.
parameters. Specify
design.
rules/contraints.

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Guide dc_shell. The
dc_shell supports two

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scripting languages -
dcsh, which uses the
Synopsys language,
and dctcl, which uses
Tcl (Tool Command
Language). It is
recommended that
Design Analyzer be
used for most of the
synthesis and
optimization processes.

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Command-Line
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RTL-to-Gates Synthesis

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```
%> dc shell -t any  
memory LIB file %>  
dc_shell dc_shell-t>  
read_lib t13spsram512  
x32_slow_syn.lib  
dc_shell-t> write_lib  
t13spsram512x32  
-output \ t13spsram512  
x32_slow_syn.db
```

Modify

```
<.synopsys_dc.setup>  
File: "*" user library  
name, which should be  
the same as the library  
name in the Artisan set
```

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link_library slow.db t13
spsram512x32_slow.db

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you're logged into your
Google Account and go
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use man compile ultra
at the DC shell prompt.
Run the following

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Design Compiler
Graphical - Synopsys
It has 2 user interfaces
:- 1) Design Vision- a GUI (Graphical User Interface) 2) dc_shell -
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a command line interface In this tutorial we will take the verilog code you have written in lab 1 for a full adder and “synthesize” it into actual logic gates using the design compiler tool.

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This command allows a macro to request input from the user. q: exits from a macro, and also from the macro which

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invoked it. If called from the top level, or from a macro which was called directly from the top level, the q command causes dc to exit. Q: Pops a value off the stack and uses it as a count of levels of macro execution to be exited.

AC/DC Magnetic Meter
- Extech Instruments

Design Compiler
Graphical extends DC
Ultra™ topographical

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technology to produce physical guidance to the IC Compiler place-and-route solution, tightening timing and area correlation to 5% while speeding-up IC Compiler placement by 1.5X.

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